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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/622,734	11/27/2000	Keisuke Koga	YAO-432US	2803

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EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/622,734	KOGA, KEISUKE	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9-13* is/are rejected.

7)☒ Claim(s) *7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

The examiner has considered the items listed in the Information Disclosure filed on 11/27/00 and entered as Paper No. 5, *except for* item 64-61953, which has not been enclosed by Applicant, nor has it been possible to acquire said item electronically. Applicant is requested to send a copy with translated abstract or abstract in English as soon as possible.

Drawings

1. Figures 8a, 8b, and 9 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

2. ***Claims 7 and 8*** are objected to because of the following informalities: in claim 7 the phrase "the shield electrode is provided in such a manner as to cover the channel region of the field effect transistor portion which is not covered with the gate electrode" should be replaced by "the shield electrode is provided in such a manner as to cover the channel region of the field effect transistor portion which is not covered with the gate electrode, while the potential of said shield electrode is made to be equal to that of the substrate". Appropriate correction is required.

Specification

The specification is objected to because nowhere in the disclosure Applicant describes or gives any details regarding location, shape or otherwise, of the p-type conductive region that is to be part of the drain region as required by claim 10.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. ***Claims 1 and 5*** are rejected under 35 U.S.C. 102(b) as being anticipated by Kuriyama et al (5, 550,435). Kuriyama et al teach (cf. Figure 3) a field emission type electron source device (cf. title and abstract) comprising:

a field emission electron source portion including an extraction electrode 2 (cf. column 4, line 38) provided on a p-type silicon substrate 5 (cf. column 4, line 39) via an insulating film 3 (cf. column 4, line 38) and having an opening portion (located around 1, see Figure 3) at a position corresponding to a region where a cathode is provided; and a cathode portion provided on the p-type silicon substrate and at a position corresponding to the opening portion of the extraction electrode; and

an n-channel field effect transistor portion (comprising IGFET gate 8, channel between source 6 and drain 4/6; cf. column 4, line 41) provided on the p-type silicon substrate, corresponding to the field emission electron source portion, wherein:

the field emission electron source portion is provided in a drain region 4/6 (cf. column 4, lines 39-40) of the field effect transistor portion; and a control voltage is applied to a gate electrode 8 (cf. column 4, line 41) of the field effect transistor portion to control a field emission current from the field emission source portion;

the drain region includes at least two wells 4 and 6 having different impurity concentrations (4 is n-doped and 6 is n+ doped silicon) (cf. column 4, lines 45-46); and

of the at least two wells, one well having a low impurity concentration is provided at an end of the drain (said drain being to the left of the channel between drain and source; cf, Figure 3) which contacts the channel region of the field effect transistor portion.

In conclusion, Kuriyama anticipates claim 1.

About claim 5: the gate insulation film between the p-silicon substrate and IGFET gate 8 is thinner than the insulating film 3 (see Figure 3). Therefore, Kuriyama et al also anticipate claim 5.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. ***Claims 2-3*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al (5, 550, 435), in view of Akamatsu et al (5,396,096).

As explained above, Kuriyama et al anticipate claim 1.

Kuriyama et al do not necessarily teach the further limitation of claim 2. However, the use of two different impurity elements having different thermal diffusivities or diffusion speeds in the silicon substrate has long been known and applied in the art of field effect transistors, as witnessed by Akamatsu et al, who teach the thermal diffusion of phosphorus and arsenic whose diffusion coefficients are different from each other, phosphorus having a high thermal diffusivity, arsenic having a relatively low thermal diffusivity in the silicon substrate 10 (this remark pertains to claim 3), thus obtaining a heavily doped part and a lightly doped part of the drain (cf. column 11, line 66 – column 12, line 3).

It is well known that the purpose of LDD (lightly doped drain) implementation is the avoidance of hot electron carrier effects (cf. column 11, lines 53-55 in loc. cit.) while the purpose of using different impurities distinct in having different thermal diffusivities is one of obvious convenience: a single heating process establishes two diffusion regions.

It is concluded that there is thus motivation to combine the references and that the long-standing success of thermal diffusion for impurity doping combined with the very different thermal diffusivities of phosphorus and arsenic justify a reasonable expectation of success.

7. ***Claim 4*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al (5,550,435), in view of Ogata (JP360022375A). Kuriyama et al teach (cf. Figure 3) a field emission type electron source device (cf. title and abstract) comprising:

a field emission electron source portion including an extraction electrode 2 (cf. column 4, line 38) provided on a p-type silicon substrate 5 (cf. column 4, line 39) via an insulating film 3 (cf. column 4, line 38) and having an opening portion (located around 1, see Figure 3) at a position corresponding to a region where a cathode is provided; and a cathode portion provided on the p-type silicon substrate and at a position corresponding to the opening portion of the extraction electrode; and

an n-channel field effect transistor portion (comprising IGFET gate 8, channel between source 6 and drain 4/6; cf. column 4, line 41) provided on the p-type silicon substrate, corresponding to the field emission electron source portion, wherein:

the field emission electron source portion is provided in a drain region 4/6 (cf. column 4, lines 39-40) of the field effect transistor portion; and a control voltage is applied to a gate electrode 8 (cf. column 4, line 41) of the field effect

transistor portion to control a field emission current from the field emission source portion.

Kuriyama et al do not necessarily teach lines 24-28 of claim 4. However, the teaching of a gate widening near the drain end of the channel so as to increase withstand voltage has long been known in the art, as evidenced by Japanese Patent to Ogata. Because any increase in withstand voltage is equivalent to an improvement in breakdown at a fixed operational voltage, the inventions of Kuriyama et al and Ogata are analogous, whence motivation to combine them exists. Furthermore, all that is necessary for a combination of the inventions is a broadening of the gate near the drain. Therefore, reasonable expectation of success is justified.

8. ***Claims 6, 9, 11-13*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al (5, 550,435) in view of Japanese Patent to Hirano et al (JP409063467A).

As detailed above, Kuriyama et al anticipate Claim 5; however, they do not necessarily teach the further limitation of Claim 6. Nevertheless, it would have been obvious to use thermal oxidation to produce the insulating film as it is understood in the art that silicon dioxide is an excellent insulating film generally in semiconductor field effect device technology while it is economically produced, given the silicon substrate suitable to provide the fuel, while Hirano et al teach the use of thermal oxidation for the more specific purpose of sharpening the tip of the cathode portion of the field emission electrode source portion of their cold cathode device (see [0034] and title and abstract).

Motivation to combine stems from the requirement of a micropoint of the electron emitter taught by Kuriyama et al (see their claim 1 for instance). Combinability of the inventions by Kuriyama et al and Hirano et al is obvious in view of the efficiency of producing said tip and gate insulating film together in this manner. Reasonable expectation of success of the combination of said inventions follows from the fact that no new steps are introduced at any stage.

With regard to claim 9: as explained above, Kuriyama et al teach the limitations of claim 9 up to and including line 18. Although Kuriyama et al do not specifically teach the limitation concerning the drain (lines 15-18), Hirano et al teach a field emission type electron source device with substantially circular borders of the drain with the emitter in the center, as seen from Figure 5, such that the drain is provided in and surrounded by the source region. Also, Figure 5 shows the gate electrode of the field effect transistor to be positioned substantially symmetrical in a plane with respect to the cathode portion of the field emission electron source portion. Although Hirano et al do not necessarily stipulate the symmetry of the configuration implied by the claim, a lack of symmetry of the configuration consisting of the emitter, the drain region as surrounded by the source region, and the gate would necessarily permit the occurrence of asymmetries in the potentials and currents, thereby necessarily and obviously leading to a lower breakdown voltage of the semiconductor portions of the device for the same level of electron flux.

With regard to claim 11: it is inherent in any channel, as defined in the art of field effect transistors, that it is a conduit between source and drain. Therefore, an outer portion of the drain region must contact the channel region of the field effect transistor

portion. Furthermore, the above-mentioned symmetry (claim 9) implies that the inner portion of the source region has concentric circles.

With regard to claim 12: combination of Figures 4 and 5 implies, with the symmetry discussed under claim 9, that the gate electrode provided between source and drain has at least a part that has a shape of a symmetrical circular arc.

With regard to claim 13: It is understood by those skilled in the art that minute gate voltages suffice to substantially change the conductivity in the channel, whence the very essence of the applicability of field effect transistors, while, as taught by Kuriyama et al, extraction voltages of the order of 10^7 V/cm are involved for electron emission (cf. column 2, lines 55-60).

9. ***Claim 10*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al and Hirano et al as applied to claim 9 above, and further in view of Bergonzoni (4,968,639). As detailed above, claim 9 is unpatentable over Kuriyama et al in view of Hirano et al, neither of whom necessarily teach the further limitation defined by claim 10. However, the inclusion of p-type conductive layers in an n-type drain has long been known by those skilled in the art of lightly-doped drain type field effect transistors as a means to combat punch-through, as witnessed by Bergonzoni, who teaches p-type layers 13' in n-type drain and source regions 31 (cf. column 2, lines 45-63). Because the purpose of the lightly-doped drain regions is relevant to the aim of Kuriyama et al to gain better control of emission the motivation to combine the references is clear. Implementation is simply achieved in the manner indicated by

Bergonzoni (loc. cit.) by lightly doped the upper region of the substrate comprising the step of thermal diffusion already pertinent to the device of claim 9 because of the existence of course and drain regions. As only an additional step similar to the step of producing source and drain is involved in the implementation of the relevant aspect of Bergonzoni, expectation of success is justifiably deemed reasonable.

Allowable Subject Matter

10. ***Claims 7 and 8*** would be allowable subject to compliance with the request for appropriate action as stated in the abovementioned objections.

11. The following is a statement of reasons for the indication of allowable subject matter: Shielding electrodes in the art of field emission type electron sources with field effect transistor, so as to cover the part of the channel not covered by the gate electrode while having the same potential as the substrate, said shielding electrodes being made of the same material as the gate, have not been found in the Prior Art to date, nor has any reason surfaced as to why such shielding electrodes should be obvious.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers

for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
May 20, 2002

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